A Novel Design and Implementation of New Double Feynman and Six-correction logic (DFSCL) gates in Quantum-dot Cellular Automata (QCA)

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Abstract

In recent years, quantum cellular automata (QCA) have been used widely to digital circuits and systems. QCA technology is a promising alternative to CMOS technology. It is attractive due to its fast speed, small area and low power consumption. The QCA offers a novel electronics paradigm for information processing and communication. It has the potential for attractive features such as faster speed, higher scale integration, higher switching frequency, smaller size and low power consumption than transistor based technology. In this paper, Double Feynman and Six-correction logic gate (DFSCL) is proposed based on QCA logic gates: MV gate and Inverter gate. The proposed circuit is a promising future in constructing of nano-scale low power consumption information processing system and can stimulate higher digital applications in QCA.

Keywords: Quantum Cellular Automata; QCA Logic Gates; DFSCL gate, dfscl gate in QCA

Introduction

Quantum technology has gradually applied in various fields (Yi Liu 2008, Hao Li, Shiyong Li: 2011). Quantum-dot cellular automata is projected as a promising nanotechnology for future *ICs* (Lent et al. 1993; Lent and Tougaw, 1997; Bahar et al. 2013a; Sarker et al. 2014). A *QCA* is an array of structures known as quantum-dots. Computing with *QCA* is achieved by the tunneling of individual electrons among the quantum-dots inside a cell and the classical coulomb interaction among them (Abdullah-Al-Shafi et al.2017; Bahar et at.2017) . A *QCA* cell consists of two electrons

positioned at opposite corners owing to columbic repulsion (Islam et at. 2014; Bahar et al. 2014; Sarker et at. 2017), so the polarization states of *P*=-1 and *P*=+1 can be represented by two stable configuration of a pair of electrons, the corresponding the logic values of "0" and "1" also be represented in Fig.1 The electrostatic repulsion between electrons leads to the synchronization of neighboring cells. Thus, one cell's polarization is determined by the effect of its neighboring cell's polarization (Al Shafi et al. 2015; Bahar et al. 2015a; Abdullah-Al-Shafi, & Bahar 2016; BAHAR, et al. 2015b)

Therefore, the array of *QCA* cells will be able to propagate information as a wire (Abdullah-Al-Shafi et al. 2015; Bahar, & Waheed 2016;). The *QCA* cells can form the primitive logic gates shown in Fig. 2 (inverter gate), Fig. 3 (majority gate). A majority gate with the logic function of *MV(A,B,C) = AB+AC+BC* is composed of five cells. By setting one of the inputs of this gate permanently to 0 or 1, *AND* and *OR* functions will be formed in *QCA*. Some other combinational logic designs with plus-shaped quantum-dot cellular automata using minority gate as the fundamental building block have been presented in (Islam et al.2016; Bahar et al. 2017).

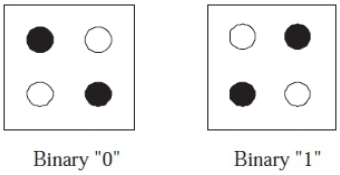


Fig.1: Quantum cellular automata

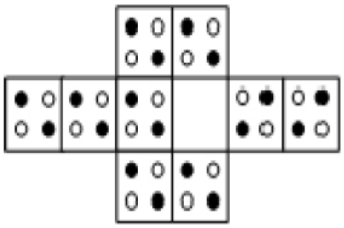


Fig.2: Inverter gate

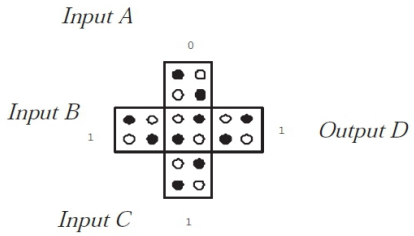


Fig.3: Majority gate

An array of cells that are aligned can construct a QCA wire which is shown in Figure 4. The polarization of each cell in a QCA wire is directly affected by the polarization of its neighboring cells on account of electrostatic force(Bahar et al. 2017; Abdullah-Al-Shafi et al. 2017). Accordingly, QCA wires can be used to propagate information from one end to another(Abdullah-Al-Shafi & Bahar 2016; Islam et al. 2015) .

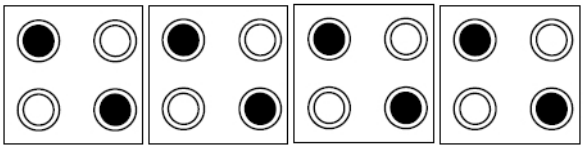


Fig. 4 A QCA Wire

Reversible Logic Gate

Six-Correction Logic Gate

Six-Correction Logic Gate is a 4 x 4 gate with two garbage outputs (Rahman et al.2015; Rahman, M. S., Waheed, S., Bahar, A. N.:2015), the input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S) and output is defined by P = A, Q = B, R = C, S=A (B+C) ⊕D the relation between input and output shown in figure 5. There is a one-to-one mapping between inputs and outputs of SCL gate and it can be used to add 6 to the sum in order to correct it to get the correct BCD sum (Bhagyalakshmi and Venkatesha : 2010).

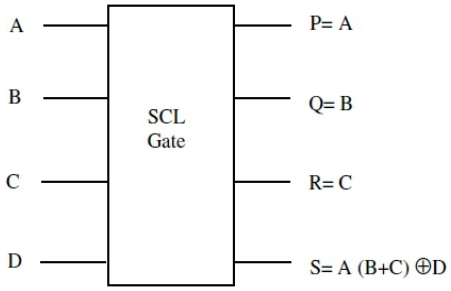


Fig.5 Six-correction logic gate (SCL)

Double Feynman gate (F2G)

Figure 6 shows a 3 x 3 Double Feynman gate (Bahar et al. 2013b; Parhami:2006). The input vector is I (A, B, C) and the output vector is O (P, Q, R) and output is defined by P = A, Q = A⊕B, R = A⊕C.

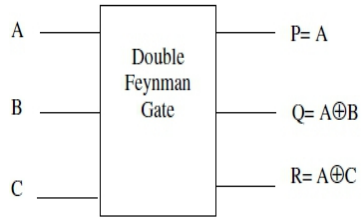


Fig.6 Double Feynman gate

Proposed dfscl gate

DFSCL gate

Figure 7 shows a DFSCL Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S).P =A, Q =A⊕B, R =A ⊕ C and S= A(B+ C) ⊕D.

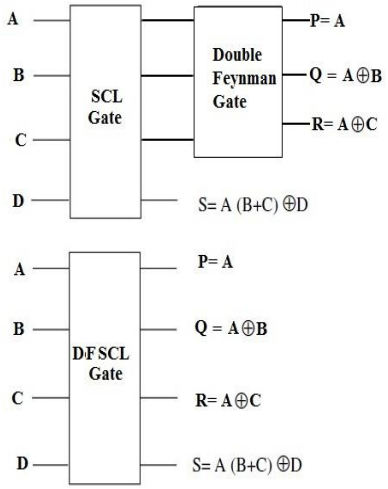


Fig.7 DFSCL Gate

Figure 8 shows the QCA representation of Six-Correction Logic Gate (DFSCL)

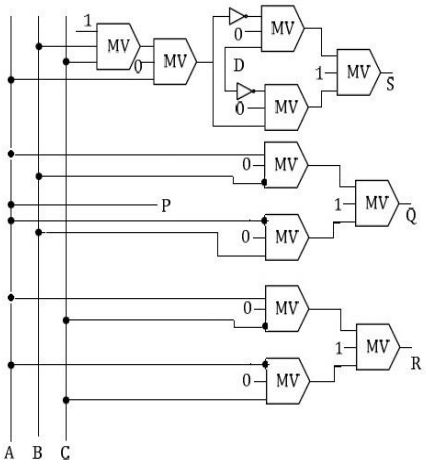
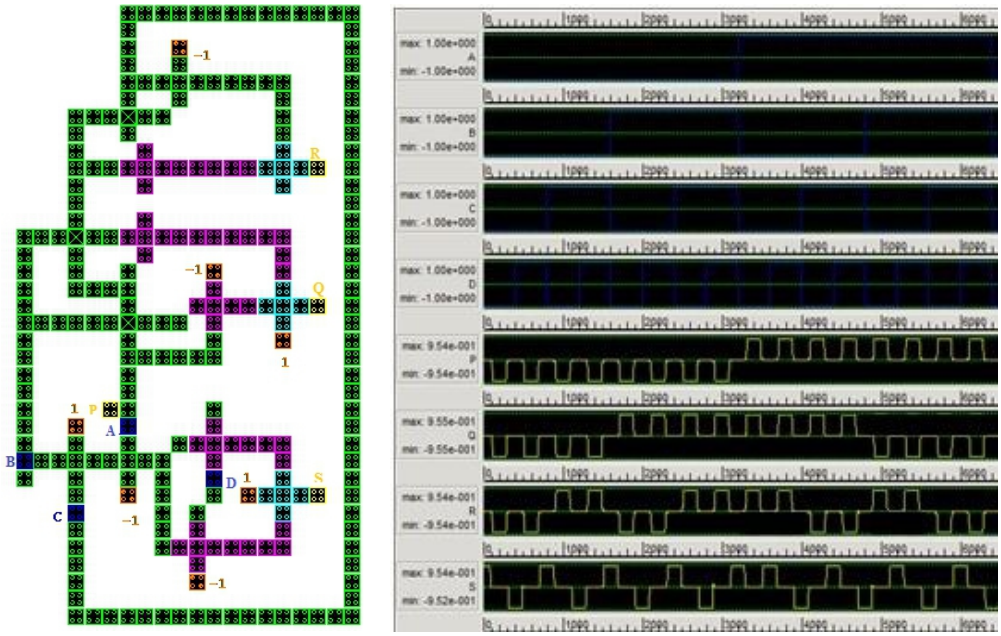


Fig.8 QCA block diagram of DFSCL gate

based of majority voter (MV) gate. Here eleven majority gates are used to design Six-correction logic gate (DFSCL).

Simulation Result and Discussion

The circuit is functionally simulated using the QCADesigner (Budiman & Dysart, Jullien, T. J., R. A., Walus, 2004). The simulated circuit layout is shown in Figure 9, here the input signals are: A, B, C and D and the output signals are: P=A, Q=A⊕B, R=A ⊕ C and S=A (B+C) ⊕D and this module goes through four clock zones, it means that the delay is a full clock cycle. Therefore, at the output P, Q, R and S are available one clock cycles after A, B, C and D has been applied. Moreover, it requires One Hundred Sixty (160) cells and total area of 0.22 μm^2.



(a) (b)

Fig.9 (a) QCA circuit layout of DFSCL logic gate and (b) simulated waveforms proposed circuit

We can find the output value of S is low level when the input digits (A = 0, B = 0, C = 0, D = 0) and S is up level when the input digits (A = 0, B =0, C= 0, D =1). We look into the other two output values of A, B and C also translating the input data successfully. The simulated waveforms of DFSCL gate is shown in figure 10. Here, the S output is delayed by 1clock cycle. Finally, in Table 1, designing parameters are compared.

Table 1. Comparison of proposed DFSCL logic circuit designs

Design	Number of Cells	Area (in μm^2)	Delay (clock cycle)
DFSCL logic circuit	160	0.22 × 1.00 = 0.22	1.00

Conlusion

This paper present New Double Feynman and Six-correction logic (DFSCL) gate based on QCA does logic gates. The proposed DFSCL gate has been simulated and verified using QCADesigner. The result is compared in terms of complexity (cell count), covered area and time delay. The simulation result shows that the proposed design achieves a sound improvement. This design will be very helpful for designing ultra low power digital circuits.

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